```
//--------------------------------------------------------------------------------
// File: KE1_tri_a.sim
//
// Description:
//   This SimFile contains the KE1 MCU simulator.
//

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//--------------------------------------------------------------------------------
//    %File_name:  KE1_tri_a.sim %
//      %Version:  8 %
//   %Created_by:  jlogue %
// %Date_created:  Tue Sep  7 07:26:32 2021 %
//--------------------------------------------------------------------------------

Signal:

  VDD                   "Sig Voltage"   // Power Inputs
  VSS                   "Sig Voltage"
  VDDA                  "Sig Voltage"
  VSSA                  "Sig Voltage"

  NMI                   "Sig Bool"      // Cortex-M4 Inputs

  _RESET_IN             "Sig Bool"      // Reset Inputs
  _RESET_OUT            "Sig Bool"      // Reset Outputs

  EXTAL                 "Sig Clock"     // Clock Inputs
  EXTAL32               "Sig Clock"
  TCLK[0:2]             "Sig Clock"
  RTC_CLKIN             "Sig Clock"
  BUSOUT                "Sig Clock"     // Clock Outputs
  CLKOUT                "Sig Clock"
  RTC_CLKOUT            "Sig Clock"

  // Note: Pins ADC1_SE[9,12:15] and ADC2_SE[8:11] not present in 64-pin KE1
  ADC[0:2]_SE[0:15]     "Sig Voltage"   // ADC Inputs
  VREFH                 "Sig Voltage"

  CMP[0:2]_IN[0:6]      "Sig Voltage"   // CMP Inputs
  CMP[0:2]_OUT          "Sig Bool"      // CMP Outputs

  REFV[1:2]             "Sig Voltage"   // DAC Inputs
  DAC0_OUT              "Sig Voltage"   // DAC Outputs

  LPSPI[0:1]_SIN        "Sig SPI"       // LPSPI Inputs
  LPSPI[0:1]_PCS[0:3]   "Sig Bool"      // LPSPI Outputs
  LPSPI[0:1]_SCK        "Sig Clock"
  LPSPI[0:1]_SOUT       "Sig SPI"

  LPI2C[0:1]_HREQ       "Sig Bool"      // LPI2C Inputs

  LPUART[0:2]_RX        "Sig RS232"     // LPUART Input
  LPUART[0:2]_TX        "Sig RS232"     // LPUART Outputs
  LPUART[0:2]_RTS       "Sig Bool"
  LPUART[0:2]_CTS       "Sig Bool"

  CAN[0:1]_RX           "Sig CAN"       // FlexCAN Inputs
  CAN[0:1]_TX           "Sig CAN"       // FlexCAN Outputs

  FTM[0:3]_FLT[0:3]     "Sig Bool"      // FTM Inputs
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  FTM[0:3]_CH[0:7]_PWM  "Sig Bool"      // FTM Outputs

  EWM_IN                "Sig Bool"      // EWM Inputs
  _EWM_OUT              "Sig Bool"      // EWM Outputs

DoubleSignal:

  PT[A:E][0:17]         "Sig Bool"      // Port Inputs

  LPI2C[0:1]_SCL        "Sig Bool"      // LPI2C I/O
  LPI2C[0:1]_SDA        "Sig Bool"
  LPI2C[0:1]_SCLS       "Sig Bool"
  LPI2C[0:1]_SDAS       "Sig Bool"
  LPI2C[0:1]_I2C        "Sig I2C"

  FXIO_D[0:7]           "Sig Bool"      // FlexIO I/O

CodedPart:

SimFilePart:

  ARM_Cortex_M4_tri_a     Cortex-M4
  KE1_System_tri_a        System
  KE1_Memory_tri_a        Memory
  KE1_Clocks_tri_a        Clocks
  KE1_Reset_tri_a         Reset
  KE1_Power_tri_a         Power
  KE1_Security_tri_a      Security
  KE1_HMI_tri_a           HMI
  KE1_Analog_tri_a        Analog
  KE1_Timers_tri_a        Timers
  KE1_Comm_tri_a          Comm
  KE1_Misc_tri_a          Misc

Connection:

  //-- Connections to Cortex-M4
  Power LOGIC_PWR                Cortex-M4 LOGIC_PWR
  Reset _CORE_RESET              Cortex-M4 _CORE_RESET
  Clocks CORE_CLK                Cortex-M4 CORE_CLK
  Clocks BUS_CLK                 Cortex-M4 BUS_CLK
  Reset PWR_RESET_TYPE           Cortex-M4 PWR_RESET_TYPE
  Reset NMI_ENAB                 Cortex-M4 NMI_ENAB
  this NMI                       Cortex-M4 NMI
  System DMA[0:15]_XFER_INT      Cortex-M4 IRQ[0:15]
  System DMA_ERR_INT             Cortex-M4 IRQ16
  System MCM_INT                 Cortex-M4 IRQ17
  Memory FTFE_CMD_INT            Cortex-M4 IRQ18
  Memory FTFE_RD_COL_INT         Cortex-M4 IRQ19
  Misc IRQ20                     Cortex-M4 IRQ20
  Memory FTFE_FAULT_INT          Cortex-M4 IRQ21
  Misc IRQ22                     Cortex-M4 IRQ22
  Comm LPI2C[0:1]_INT            Cortex-M4 IRQ[24:25]
  Comm LPSPI[0:1]_INT            Cortex-M4 IRQ[26:27]
  Timers PWT_INT                 Cortex-M4 IRQ29
  Comm LPUART0_TX_INT            Cortex-M4 IRQ31
  Comm LPUART0_RX_INT            Cortex-M4 IRQ32
  Comm LPUART1_TX_INT            Cortex-M4 IRQ33
  Comm LPUART1_RX_INT            Cortex-M4 IRQ34
  Comm LPUART2_TX_INT            Cortex-M4 IRQ35
  Comm LPUART2_RX_INT            Cortex-M4 IRQ36
  Analog ADC0_INT                Cortex-M4 IRQ39
  Analog CMP[0:1]_INT            Cortex-M4 IRQ[40:41]
  Timers FTM[0:2]_INT            Cortex-M4 IRQ[42:44]
  Timers RTC_TIME_INT            Cortex-M4 IRQ46
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Timers RTC_SECS_INT             Cortex-M4 IRQ47
Timers LPIT0_CH[0:3]_INT        Cortex-M4 IRQ[48:51]
Timers PDB0_INT                 Cortex-M4 IRQ52
Analog DAC0_INT                 Cortex-M4 IRQ56
Misc IRQ57                      Cortex-M4 IRQ57
Timers LPTMR0_INT               Cortex-M4 IRQ58
HMI PORT[A:E]_INT               Cortex-M4 IRQ[59:63]
Timers PDB1_INT                 Cortex-M4 IRQ68
Comm FLEXIO_INT                 Cortex-M4 IRQ69
Analog CMP2_INT                 Cortex-M4 IRQ70
Timers FTM3_INT                 Cortex-M4 IRQ71
Analog ADC[1:2]_INT             Cortex-M4 IRQ[73:74]
Timers PDB2_INT                 Cortex-M4 IRQ77
Comm CAN0_OR_MB_INT             Cortex-M4 IRQ78
Comm CAN0_ERR_INT               Cortex-M4 IRQ79
Comm CAN0_WAKE_INT              Cortex-M4 IRQ80
Comm CAN0_OR_MB_INT             Cortex-M4 IRQ81
Comm CAN0_RESV[1:3]_INT         Cortex-M4 IRQ[82:84]
Comm CAN1_OR_MB_INT             Cortex-M4 IRQ85
Comm CAN1_ERR_INT               Cortex-M4 IRQ86
Comm CAN1_WAKE_INT              Cortex-M4 IRQ87
Comm CAN1_OR_MB_INT             Cortex-M4 IRQ88
Comm CAN1_RESV[1:3]_INT         Cortex-M4 IRQ[89:91]

//-- Connectins to part edge from Cortex-M4

//-- Connections to System
Power LOGIC_PWR                 System LOGIC_PWR
Reset _SYS_RESET                System _SYS_RESET
Clocks BUS_CLK                  System BUS_CLK
Clocks SYS_CLK                  System SYS_CLK
Clocks SOSC_CLK                 System SOSC_CLK
Clocks OSC32_CLK                System OSC32_CLK
Clocks MPU_PI_CLK               System MPU_PI_CLK
Clocks SCG_CLKOUT               System CLKOUT
Power LPO_CLK                   System LPO_CLK
this TCLK[0:2]                  System TCLK[0:2]
this RTC_CLKIN                  System RTC_CLKIN

Cortex-M4 PUSH_ISCR             System CATCH_ISCR   // To MCM

Timers RTC_SECOND               System RTC_SECOND   // To TRGMUX0
Timers RTC_ALARM                System RTC_ALARM
Timers LPTMR0_TRG               System LPTMR0_TRG
Timers LPIT0_CH[0:3]_TRG        System LPIT0_CH[0:3]_TRG
Timers FTM[0:3]_TRG             System FTM[0:3]_TRG
Analog ADC[0:2]_COCO[A:B]_TRG   System ADC[0:2]_COCO[A:B]_TRG
Analog CMP[0:2]_OUT_TRG         System CMP[0:2]_OUT_TRG
Comm FLEXIO_TRG[0:3]            System FLEXIO_TRG[0:3]

this VDD                        System VDD          // To TRGMUX1
this VSS                        System VSS
System SIM_SW_TRG               System SIM_SW_TRG
Comm LPUART[0:1]_RX_DATA        System LPUART[0:1]_RX_DATA
Comm LPUART[0:1]_TX_DATA        System LPUART[0:1]_TX_DATA
Comm LPUART[0:1]_RX_IDLE        System LPUART[0:1]_RX_IDLE
Comm LPI2C[0:1]_MASTER_STOP     System LPI2C[0:1]_MASTER_STOP
Comm LPI2C[0:1]_SLAVE_STOP      System LPI2C[0:1]_SLAVE_STOP
Comm LPSPI[0:1]_FRAME           System LPSPI[0:1]_FRAME
Comm LPSPI[0:1]_RX_DATA         System LPSPI[0:1]_RX_DATA

Clocks DMAMUX0_PI_CLK           System DMAMUX0_PI_CLK   // To DMAMUX
Comm LPUART[0:2]_DMA_REQ_RX     System LPUART[0:2]_DMA_REQ_RX
Comm LPUART[0:2]_DMA_REQ_TX     System LPUART[0:2]_DMA_REQ_TX
Comm FLEXIO_DMA_REQ[0:3]        System FLEXIO_DMA_REQ[0:3]
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Comm LPSPI[0:1]_DMA_REQ_RX      System LPSPI[0:1]_DMA_REQ_RX
Comm LPSPI[0:1]_DMA_REQ_TX      System LPSPI[0:1]_DMA_REQ_TX
Comm LPI2C[0:1]_DMA_REQ_RX      System LPI2C[0:1]_DMA_REQ_RX
Comm LPI2C[0:1]_DMA_REQ_TX      System LPI2C[0:1]_DMA_REQ_TX
Timers FTM[0:3]_DMA_REQ[0:7]    System FTM[0:3]_DMA_REQ[0:7]
Analog ADC[0:2]_DMA_REQ         System ADC[0:2]_DMA_REQ
Analog CMP[0:2]_DMA_REQ         System CMP[0:2]_DMA_REQ
Timers PDB[0:2]_DMA_REQ         System PDB[0:2]_DMA_REQ
HMI PORT[A:E]_DMA_REQ           System PORT[A:E]_DMA_REQ
Comm CAN[0:1]_DMA_REQ           System CAN[0:1]_DMA_REQ
Analog DAC0_DMA_REQ             System DAC0_DMA_REQ
Timers LPTMR0_DMA_REQ           System LPTMR0_DMA_REQ

Clocks DMA0_PI_CLK              System DMA0_PI_CLK      // To eDMA

Timers PDB[0:2]_DAC             System PDB[0:2]_DAC
Timers PDB[0:2]_PULSE           System PDB[0:2]_PULSE

Cortex-M4 PRIV_EN               System PRIV_EN

//-- Connections to part edge from System

//-- Connections to Memory
Power LOGIC_PWR               Memory LOGIC_PWR
Power LOGIC_PWR3              Memory LOGIC_PWR3
Reset _CORE_RESET             Memory _CORE_RESET
Reset _SYS_RESET              Memory _SYS_RESET
Clocks SYS_CLK                Memory SYS_CLK
Clocks BUS_CLK                Memory BUS_CLK
Clocks FLASH_CLK              Memory FLASH_CLK
Reset READ_FOPT               Memory READ_FOPT
System SRAM_L_WR_PROT         Memory SRAM_L_WRITE_PROTECT
System SRAM_U_WR_PROT         Memory SRAM_U_WRITE_PROTECT

//-- Connections to part edge from Memory

//-- Connections to Clocks
Power LOGIC_PWR               Clocks LOGIC_PWR
Reset _SYS_RESET              Clocks _SYS_RESET
Power RUN_MODE                Clocks RUN_MODE
Memory FOPT                   Clocks FOPT
Timers RTC_OSCE               Clocks RTC_OSCE
this EXTAL                    Clocks EXTAL
this EXTAL32                  Clocks EXTAL32
Analog ADC[0:2]_INUSE         Clocks ADC[0:2]_INUSE
Analog CMP[0:2]_INUSE         Clocks CMP[0:2]_INUSE
Analog DAC0_INUSE             Clocks DAC0_INUSE
Comm CAN[0:1]_INUSE           Clocks CAN[0:1]_INUSE
Comm FLEXIO_INUSE             Clocks FLEXIO_INUSE
Comm LPI2C[0:1]_INUSE         Clocks LPI2C[0:1]_INUSE
Comm LPSPI[0:1]_INUSE         Clocks LPSPI[0:1]_INUSE
Comm LPUART[0:2]_INUSE        Clocks LPUART[0:2]_INUSE
HMI PORT[A:E]_INUSE           Clocks PORT[A:E]_INUSE
Memory FLASH_INUSE            Clocks FLASH_INUSE
Security CRC_INUSE            Clocks CRC_INUSE
Security EWM_INUSE            Clocks EWM_INUSE
System DMA0_INUSE             Clocks DMA0_INUSE
System DMAMUX0_INUSE          Clocks DMAMUX0_INUSE
System MPU_INUSE              Clocks MPU_INUSE
Timers FTM[0:3]_INUSE         Clocks FLEXTMR[0:3]_INUSE
Timers LPIT0_INUSE            Clocks LPIT0_INUSE
Timers LPTMR0_INUSE           Clocks LPTMR0_INUSE
Timers PDB[0:2]_INUSE         Clocks PDB[0:2]_INUSE
Timers PWT_INUSE              Clocks PWT_INUSE
Timers RTC_INUSE              Clocks RTC_INUSE
```

```
//-- Connections to part edge from Clocks
Clocks BUS_CLK                this BUSOUT

//-- Connections to Reset
Power LOGIC_PWR               Reset LOGIC_PWR
this  _RESET_IN               Reset _RESET_IN
Clocks BUS_CLK                Reset BUS_CLK
Power LPO_CLK                 Reset LPO_CLK
Memory FOPT                   Reset FOPT
Power _LVD_RESET              Reset _LVD_RESET
Security WDOG_RESET           Reset WDOG_RESET
Clocks SPLL_LOL_RESET         Reset SPLL_LOL_RESET
Clocks SOSC_LOC_RESET         Reset SOSC_LOC_RESET
Cortex-M4 SW_RESET            Reset SW_RESET
Cortex-M4 LOCKUP_RESET        Reset LOCKUP_RESET

//-- Connections to part edge from Reset
Reset _RESET_OUT              this _RESET_OUT

//-- Connections to Power
this VDD                      Power VDD
this VSS                      Power VSS
Reset _SYS_RESET              Power _SYS_RESET
Clocks BUS_CLK                Power BUS_CLK

//-- Connections to part edge from Power

//-- Connections to Security
Power LOGIC_PWR               Security LOGIC_PWR
Reset _SYS_RESET              Security _SYS_RESET
Clocks BUS_CLK                Security BUS_CLK
Clocks SOSC_CLK               Security SOSC_CLK
Clocks SIRC_CLK               Security SIRC_CLK
Clocks EWM_PI_CLK             Security EWM_PI_CLK
Clocks CRC_PI_CLK             Security CRC_PI_CLK
Power LPO_CLK                 Security LPO_CLK
Cortex-M4 CORE_ON_EV          Security CORE_ON_EV
this EWM_IN                   Security EWM_IN

//-- Connections to part edge from Security
Security _EWM_OUT             this _EWM_OUT

//-- Connections to HMI
this VDD                      HMI VDD
this VSS                      HMI VSS
Power LOGIC_PWR               HMI LOGIC_PWR
Reset _SYS_RESET              HMI _SYS_RESET
Clocks SYS_CLK                HMI SYS_CLK
Clocks BUS_CLK                HMI BUS_CLK
Clocks PORT[A:E]_PI_CLK       HMI PORT[A:E]_PI_CLK
Power LPO_CLK                 HMI LPO_CLK

//-- Connections to part edge from HMI

//-- Connections to Analog
this VDDA                     Analog VDDA
this VSSA                     Analog VSSA
Power LOGIC_PWR               Analog LOGIC_PWR
Reset _SYS_RESET              Analog _SYS_RESET
Clocks BUS_CLK                Analog BUS_CLK
System ADC[0:2]_TRG           Analog ADC[0:2]_TRG
System ADC[0:2]_PRETRG[0:3]   Analog ADC[0:2]_PRETRG[0:3]
Timers PDB[0:2]_ADCx_TRG          Analog PDBx_ADC[0:2]_TRG
Timers PDB[0:2]_ADCx_PRETRG[0:7]  Analog PDBx_ADC[0:2]_PRETRG[0:7]
```

```
  Clocks ADC[0:2]_PI_CLK        Analog ADC[0:2]_PI_CLK
  Clocks ADC[0:2]_CLK           Analog ADC[0:2]_CLK
  this ADC[0:2]_SE[0:15]        Analog ADC[0:2]_SE[0:15]
//X   TEMP_SENSOR_V             Analog TEMP_SENSOR_V
//X   BANDGAP_1V_REF            Analog BANDGAP_1V_REF
  this VREFH                    Analog VREFH
  this VSS                      Analog VREFL
  this REFV1                    Analog REFV1
  this REFV2                    Analog REFV2
  this CMP[0:2]_IN[0:6]         Analog CMP[0:2]_IN[0:6]
  Clocks CMP[0:2]_PI_CLK        Analog CMP[0:2]_PI_CLK
  Clocks DAC0_PI_CLK            Analog DAC0_PI_CLK
  Analog CMP[0:2]_SAMPLE        Analog CMP[0:2]_SAMPLE
  System ADC_[0:2]_PRETRG_SEL   Analog ADC[0:2]_PRETRG_SEL
  System ADC_[0:2]_SW_PRETRG    Analog ADC[0:2]_SW_PRETRG
  System ADC_[0:2]_TRG_SEL      Analog ADC[0:2]_TRG_SEL
  System ADC_PTB14_INTLV_EN     Analog ADC_PTB14_INTLV_EN
  System ADC_PTB13_INTLV_EN     Analog ADC_PTB13_INTLV_EN
  System ADC_PTB1_INTLV_EN      Analog ADC_PTB1_INTLV_EN
  System ADC_PTB0_INTLV_EN      Analog ADC_PTB0_INTLV_EN

  //-- Connections to part edge from Analog
  Analog DAC0_OUT               this DAC0_OUT
  Analog CMP[0:2]_OUT           this CMP[0:2]_OUT

  //-- Connections to Timers
  Power LOGIC_PWR               Timers LOGIC_PWR
  Reset _SYS_RESET              Timers _SYS_RESET
  Clocks SYS_CLK                Timers SYS_CLK
  Clocks PDB[0:2]_PI_CLK        Timers PDB[0:2]_PI_CLK
  System PDB_BB_SEL             Timers PDB_BB_SEL
  System PDB[0:2]_TRG           Timers PDB[0:2]_TRG
  Analog ADC[0:2]_COCO[A:H]_TRG Timers ADC[0:2]_COCO[A:H]_TRG
  Clocks FLEXTMR[0:3]_PI_CLK    Timers FTM[0:3]_PI_CLK
  Clocks FLEXTMR[0:3]_CLK       Timers FTM[0:3]_CLK
  System FTM[0:3]_TCLK          Timers FTM[0:3]_TCLK
  System FTM[0:3]_HW_TRG        Timers FTM[0:3]_HW_TRG
  System FTM[0:3]_FAULT[0:2]    Timers FTM[0:3]_FAULT[0:2]
  System FTM3_OUTSEL            Timers FTM3_OUTSEL
  System FTM0_OUTSEL            Timers FTM0_OUTSEL
  System FTM2_CH1_SEL           Timers FTM2_CH1_SEL
  System FTM2_CH0_SEL           Timers FTM2_CH0_SEL
  System FTM1_CH0_SEL           Timers FTM1_CH0_SEL
  System FTM[0:3]_SYNC_BIT      Timers FTM[0:3]_SYNC_BIT
  this FTM[0:3]_FLT[0:3]        Timers FTM[0:3]_FLT[0:3]
  System FTM[0:3]_FLT[0:2]_SEL  Timers FTM[0:3]_FLT[0:2]_SEL
  Clocks LPIT0_PI_CLK           Timers LPIT0_PI_CLK
  Clocks LPIT0_CLK              Timers LPIT0_CLK
  System LPIT0_TRG_CH[0:3]      Timers LPIT0_TRG_CH[0:3]
  Clocks PWT_PI_CLK             Timers PWT_PI_CLK
  System PWT_TCLK               Timers PWT_TCLK
  System LPTMR0_ALT0            Timers LPTMR0_ALT0
  System PWT_IN0                Timers PWT_IN0
  Clocks LPTMR0_PI_CLK          Timers LPTMR0_PI_CLK
  Clocks LPTMR0_CLK             Timers LPTMR0_CLK
  Power LPO_CLK                 Timers LPO_CLK
  Clocks OSC32_CLK              Timers OSC32_CLK
  Clocks RTC_PI_CLK             Timers RTC_PI_CLK
  Power LPO_1K_CLK              Timers LPO_1K_CLK

  //-- Connections to part edge from Timers
  Timers FTM[0:3]_CH[0:7]_PWM   this FTM[0:3]_CH[0:7]_PWM
  Timers RTC_CLKOUT             this RTC_CLKOUT

  //-- Connections to Comm
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```
  Power LOGIC_PWR               Comm LOGIC_PWR
  Reset _SYS_RESET              Comm _SYS_RESET
  Clocks LPSPI[0:1]_PI_CLK      Comm LPSPI[0:1]_PI_CLK
  Clocks LPSPI[0:1]_CLK         Comm LPSPI[0:1]_CLK
  this LPSPI[0:1]_SIN           Comm LPSPI[0:1]_SIN
  System LPSPI[0:1]_TRG         Comm LPSPI[0:1]_TRG
  Clocks LPI2C[0:1]_PI_CLK      Comm LPI2C[0:1]_PI_CLK
  Clocks LPI2C[0:1]_CLK         Comm LPI2C[0:1]_CLK
  this LPI2C[0:1]_HREQ          Comm LPI2C[0:1]_HREQ
  System LPI2C[0:1]_TRG         Comm LPI2C[0:1]_TRG
  Clocks LPUART[0:2]_PI_CLK     Comm LPUART[0:2]_PI_CLK
  Clocks LPUART[0:2]_CLK        Comm LPUART[0:2]_CLK
  this LPUART[0:2]_RX           Comm LPUART[0:2]_RX
  System LPUART[0:1]_TRG        Comm LPUART[0:1]_TRG
  Clocks FLEXIO_PI_CLK          Comm FLEXIO_PI_CLK
  Clocks FLEXIO_CLK             Comm FLEXIO_CLK
  System FLEXIO_TRG_TIM[0:3]    Comm FLEXIO_EXT_TRG[0:3]
  Clocks CAN[0:1]_PI_CLK        Comm CAN[0:1]_PI_CLK
  Clocks SOSCDIV2_CLK           Comm SOSCDIV2_CLK
  this CAN[0:1]_RX              Comm CAN[0:1]_RX

  //-- Connections to part edge from Comm
  Comm LPSPI[0:1]_PCS[0:3]      this LPSPI[0:1]_PCS[0:3]
  Comm LPSPI[0:1]_SCK           this LPSPI[0:1]_SCK
  Comm LPSPI[0:1]_SOUT          this LPSPI[0:1]_SOUT
  Comm CAN[0:1]_TX              this CAN[0:1]_TX
  Comm LPUART[0:2]_TX           this LPUART[0:2]_TX
  Comm LPUART[0:2]_RTS          this LPUART[0:2]_RTS
  Comm LPUART[0:2]_CTS          this LPUART[0:2]_CTS

  //-- Connections to Misc
  Power LVD_INT                 Misc LVD_INT
  Power LVW_INT                 Misc LVW_INT
  Security WDOG_INT             Misc WDOG_INT
  Security EWM_INT              Misc EWM_INT
  Clocks SPLL_LOL_INT           Misc SPLL_LOL_INT
  Clocks SOSC_LOC_INT           Misc SOSC_LOC_INT
  Reset RCM_INT                 Misc RCM_INT

  //-- Connections to part edge from Misc

DoubleConnection:

  //-- Connections to/from Comm
  this LPI2C[0:1]_SCL           Comm LPI2C[0:1]_SCL
  this LPI2C[0:1]_SDA           Comm LPI2C[0:1]_SDA
  this LPI2C[0:1]_SCLS          Comm LPI2C[0:1]_SCLS
  this LPI2C[0:1]_SDAS          Comm LPI2C[0:1]_SDAS

  this FXIO_D[0:7]              Comm FXIO_D[0:7]

  //-- Connections to/from HMI
  this PT[A:E][0:17]            HMI PT[A:E][0:17]

AddressDataGroup:

  DataBusADG

AddressDataGroupArg:

  Cortex-M4   DataBusADG
  System      DataBusADG
  Memory      DataBusADG
  Clocks      DataBusADG
  Reset       DataBusADG
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  Power       DataBusADG
  Security    DataBusADG
  HMI         DataBusADG
  Analog      DataBusADG
  Timers      DataBusADG
  Comm        DataBusADG

AddressAmbig:

AddressRange:

StringArg:

LongIntArg:

DoubleArg:
```